Instruction Manual

Tektronix

TMS822
UTOPIA1/UTOPIA2 Software Support

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www.tektronix.com

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Preface

This instruction manual contains specific information about the TMS822 UTOPIA2 software support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating bus support packages on the logic analyzer for which the TMS822 UTOPIA2 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating bus support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of bus support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of logic analyzer online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the target system
- Setting up the logic analyzer to acquire data from the target system
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into header and payload information.
- The phrase “information on basic operations” refers to logic analyzer online help or a user manual, covering the basic operations of the bus support.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

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Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TMS822 UTOPIA2 bus support, and information on connecting your logic analyzer to your target system.

Support Package Description

The TMS822 bus support package displays disassembled data from systems based on Utopia Level 2 bus in the Transmit or Receive mode.

The highlights of Utopia Level 2 specification are as follows:

- Allows an 8-bit wide data path, using an octet-level handshake, operating up to 25 MHz, with a single PHY device.
- Allows an 8-bit wide data path, using a cell-level handshake, operating up to 25 MHz with a single PHY device.
- Defines a 33 MHz data path interface operation, intended to simplify PCI Bus ATM layer designs. This clock rate is used both with 8 and 16-bit wide data paths. The 8-bit and 16-bit wide data path cell formats conform to the specifications described in the Level 1 document.
- Defines a 50 MHz data path interface operation, intended for a 16-bit interface at line rates of 622 Mbps.
- Defines the 'physical' operation of up to n PHY devices for the Multi-PHY (MPHY) operation for the:
  - $n \leq 8$ at ATM layers intended for 155 Mbps;
  - $n \leq 4$ at ATM layers intended for 622 Mbps with virtual space set up for $n \leq 31$ PHY ports.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS822 support.

Since UTOPIA2 is backward compatible, the TMS822 support package can be used to acquire cycles from UTOPIA Level 1 system also.

The highlights of Utopia Level 1 specifications are as follows:

- UTOPIA Level 1 defines the interface between the Physical (PHY) and upper layer modules such as the ATM Layer.

- UTOPIA Level 1 supports

  Rates from 100 Mbps to 155 Mbps with a 8-bit wide data path
  Higher rates (for example 622 Mbps) with a 16-bit wide data path

To use this support efficiently, you need the items listed in the information on basic operations in your logic analyzer online help and the following user manuals for reference.

- *Utopia Level 2, Version 1.0 af-phy-0039.000 June 1995 (ATM-PHY interface specification issued by ATM Forum)*
- *ITU-T recommendation I.361 for the interpretation of the ATM cell header information*
- *ITU-T I.363 B-ISDN ATM Adaptation Layer (AAL) Specification*
- *ITU-T I.363.1 B-ISDN ATM Adaptation Layer Specification: Type 1 AAL*
- *ITU-T I.363.2 B-ISDN ATM Adaptation Layer Specification: Type 2 AAL*
- *ITU-T I.363.3 B-ISDN ATM Adaptation Layer Specification: Type 3/4 AAL*
- *ITU-T I.363.5 B-ISDN ATM Adaptation Layer Specification: Type 5AAL*
- *Transwitch data sheet for UTOPIA Level 2 plus*
- *UTOPIA Specification Level 1, Version 2.01 af-phy-0017.000, March 21, 1994*

Logic Analyzer Software Compatibility

The label on the bus support floppy disk states which version of logic analyzer software this support is compatible with.

Logic Analyzer Configuration

The TMS822 support allows a choice of required minimum module configurations.

The Utopia Level 2 support package is divided into two support packages:

- UTOPIA2RX: UTOPIA2RX requires at least one 34 channel module to acquire data from the receive interface.
- UTOPIA2TX: UTOPIA2TX requires at least one 34 channel module to acquire data from the transmit interface.

To monitor both interfaces simultaneously (if both interfaces have a common clock), the support requires two 34 channel modules. You must load the Transmit support package in one of the 34 channel modules and the Receive support package in the other. By double probing the common clock, the support acquires the Transmit and Receive data information coming on the Utopia interface simultaneously.

To use both supports (Transmit Interface and Receive Interface) at the same time, the support requires two modules. To use only one support at a time, you must select the correct module and specify the support.

Requirements and Restrictions

Review the electrical specifications in the *Specifications* section in this manual as they pertain to your target system, as well as the following descriptions of other TMS822 UTOPIA2 support requirements and restrictions.

Hardware Reset. If a hardware reset occurs in your TMS822 UTOPIA2 system during an acquisition, the application disassembler might acquire an invalid sample.

Clock Rate. The TMS822 UTOPIA2 bus support can acquire data from the TMS822 UTOPIA2 bus operating at speeds of up to 50 MHz[1]. The TMS822 UTOPIA2 bus support has been tested to 16.7 MHz.

Setup and Hold Time Adjustments. You cannot change the setup and hold time for any signal group.

Nonintrusive Acquisition. Acquiring Utopia2 bus cycles is nonintrusive to the target system. That is, the TMS822 UTOPIA2 does not intercept, modify, or present signals back to the target system.

Channel Groups. Channel groups required for clocking and disassembly for TMS822 UTOPIA2 bus support are as follows:

Receive bus:
Address Group, Data Group, Control Group, RXCLAV Group, and L2PControl Group.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Transmit bus:
Address Group, Data Group, Control Group, TXCLAV Group, and L2PControl Group.

UTOPIA Level 2 Plus. TMS822 UTOPIA2 support, when used with the Utopia Level 2 plus does not decode the acquired PPP packets. The acquired information is displayed and the disassembly identifies the packets.

Address Display. The address of the PHY port from which the cell is transmitted or received is correct only when the custom clocking option is ATM Cells/PPP Packets or ATM Cell Headers (5-bytes) option. The support displays the address only when more than one physical device is involved. In a Single PHY operation, the Address column is dashed out.

Trigger Programs. The Trigger Programs that are provided do not work when ATM cells have Extended Header Bytes.

The disassembly shows correct information only when the appropriate disassembly and custom clocking options are chosen.

Table 1–1 shows the invalid combinations of disassembly and clocking option.

Table 1–1: Invalid disassembly and clocking combinations

Clocking option	Disassembly option
All Cycles	Polling Cycles
ATM Cells/PPP Packets	All Utopia Cycles, All UtopiaL2p Cycles, Polling Cycles
ATM Cell Headers(5-bytes)	All Utopia Cycles, All UtopiaL2p Cycles, ATM Cells, PPP Packets, Polling Cycles
Polling Cycles The Number of PHY Ports must not be set to SIGPHY	All Utopia Cycles, All UtopiaL2p Cycles, ATM Cells, PPP Packets, ATM Cell Headers

AAL Decoding. This information covers the features that are supported in each of the AAL layers and their limitations.

***NOTE**. You can see AAL decoding only when the disassembly SHOW option is set to ATM Cells. All field values that are decoded are in binary. The support does not decode AAL when all the 48 payload bytes of the ATM cell are not available.*

AAL 1: In this layer, the TMS822 UTOPIA2 support decodes till the SAR-PDU level: SAR-PDU header and payload information.

Refer to the ITU-T I.363.1 B-ISDN ATM adaptation layer specification for details about the PDU format.

Limitation: The TMS822 UTOPIA2 does not support the Structured Data Transfer format of SAR-PDU payload.

AAL 2: In this layer, the TMS822 UTOPIA2 support decodes information up to the CPS-PACKET level. The support identifies the CPS-PACKET header and Packet payloads.

Refer to the ITU-T I.363.2 B-ISDN ATM adaptation layer specification for details about the PDU format.

Limitation: The TMS822 UTOPIA2 does not support multiplexing and packing of CPS-PACKETs into CPS-PDUs.

AAL 3/4: The TMS822 UTOPIA2 support decodes information up to the SAR-PDU and to a certain extent the CPCS-PDU. The support decodes the SAR-PDU to show details of the SAR-PDU Header and Trailer information and identifies the SAR-PDU as to whether it is BOM, COM, EOM, or SSM.

The support identifies the two types of SAR-PDUs namely, Data-SAR-PDU and Abort-SAR-PDU. The SAR-PDUs are further decoded to show the CPCS-PDU header and trailer information based on whether it is BOM, EOM, COM, or SSM.

Refer to the ITU-T I.363.3 B-ISDN ATM adaptation layer specification for details about the PDU format.

AAL 5: The support decodes the information up to the SAR-PDU and identifies the last SAR-PDU payload based on the AUU parameter. The support decodes the CPCS trailer information (the CPCS trailer is in the last 8 octets of the last SAR-PDU.)

Refer to the ITU-T I.363.5 B-ISDN ATM adaptation layer specification for details about the PDU format.

UTOPIA Level 1 Cycles. UTOPIA1 does not support Extended Header Bytes. For correct disassembly, set the the disassembly option ‘Extended Header Bytes’ to zero.

UTOPIA1 does not support the MULPHY scheme — Direct Status Indication. For correct disassembly, do not set the clocking and disassembly option ‘Number of PHY Ports’ to MULPHY-DSI.

Timing Display Format

A Timing Display Format file is also provided for this support. It sets up the display to show the following waveforms for the TMS822 bus support.

For UTOPIA2TX Support:

TxClk
TxFull*/TxClav
TxSOC
TxEnb*
Address
Data
Control

For UTOPIA2RX Support:

RxClk
RxEmpty*/RxClav
RxSOC
RxEnb*
Address
Data
Control

***NOTE**. An asterisk (*) following a signal name indicates an active low signal.*

Address, Data and Control groups are displayed in bus form.

Functionality Not Supported

- The appendices (1 and 2) mentioned here are described as a part of ATM Forum specification Utopia Level 2, Version 1.0 af-phy-0039.000 June 1995 (ATM-PHY interface). The software does not support the implementation of the guidelines described in these appendices.

  Appendix 1. Method to support a larger number of PHYs
  Appendix 2. Management Interface

- The TMS822 UTOPIA2 support when used with Utopia Level 2 Plus does not decode the acquired PPP packets. The support only displays the acquired information and the disassembly just identifies the packets.

- The ATM payload is not analyzed to decode higher layer protocols other than AAL.

Functionality Supported but Not Tested

The TMS822 supports the following features but they are not tested.

- Disassembling the 16-bit Data Bus width
- Decoding the AAL1, AAL2, AAL3/4, AAL 5 Layers
- Decoding the ATM cell with Extended Header Bytes
- Decoding of ATM cells from Multi-PHY Interface (namely Multi PHY-POLLING and Multi PHY-DSI)
- Decoding of the ATM cells with UNI (User Network Interface) and NNI (Network Node Interface)
- Decoding of packets from the UTOPIA Level 2 Plus Interface

These features were verified using simulated test patterns only.

Connecting the Logic Analyzer to a Target System

You can use the channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make the connections between the logic analyzer and your target system.

To connect the probes to TMS822 UTOPIA2 signals in the target system using a test clip, follow these steps:

1. Power off your target system. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the target systems, probes, and the logic analyzer module in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the target system.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored electricity from the test clip.

CAUTION. *To prevent permanent damage to the pins on the microprocessor, place the target system on a horizontal surface before connecting the test clip.*

3. Place the target system on a horizontal, static-free surface.
4. Use Tables 3–5 through 3–16 starting on page 3–3 to connect the channel probes to TMS822 UTOPIA2 signal pins on the test clip or in the target system.
5. Use leadsets to connect at least one ground lead from each channel and the ground lead from each clock probe to the ground pins on your test clip.

Labeling P6434 Probes

The TMS822 bus support package relies on the channel mapping and labeling scheme for the P6434 Probes. Apply labels using the instructions described in the P6434 Probe Instructions manual.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support and covers the following topics:

- Channel group definitions
- Clocking options

The information in this section is specific to the operations and functions of the TMS822 UTOPIA2 support on any Tektronix logic analyzer for which the support can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and display disassembled data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change the setups as needed.

Installing the Support Software

***NOTE**. Before you install any software, it is recommended you verify that the bus support software is compatible with the logic analyzer software.*

To install the TMS822 UTOPIA2 software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, follow the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

Support Package Setups

The software installs two support package setup files. Each setup file offers different clocking and display options.

Acquisition Setup. The support package consists of two different supports, one for the Transmit Interface and the other for the Receive Interface. You must make connections and load the appropriate package for the desired support. The TMS822 support will affect the logic analyzer setup menus (and submenus) by modifying existing fields, and adding UTOPIA2 bus-specific fields. The TMS822 adds the selection 'UTOPIA2RX' to the 'Load Support Package' dialog box, under the File pulldown menu when the support package for the Receive Interface is loaded.

On the logic analyzer, the TMS822 support adds the selection'UTOPIA2TX' to the 'Load Support Package' dialog box, under the File pulldown menu when the support package for the Transmit Interface is loaded. Once the corresponding support has been loaded, the 'Custom' clocking mode selection in the logic analyzer setup menu is also enabled. 'Custom' is the default selection whenever the 'UTOPIA2TX' or 'UTOPIA2RX' support loads.

***NOTE**. This procedure is applicable for acquisitions from UTOPIA Level 1 systems also.*

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS822 UTOPIA2 support for the Receive bus are Address, Data, Control, RXCLAV, Parity and L2PControl.

Table 2-1: Receive bus group names

Group name	Display radix
Address	HEX
Data	HEX
Mnemonics	NONE - Disassembly generated text
Control	SYM
RXCLAV	BIN
Parity	BIN
L2PControl	SYM

The channel groups for the TMS822 UTOPIA2 support for the Transmit bus are Address, Data, Control, TXCLAV, Parity and L2PControl.

Table 2-2: Transmit bus group names

Group name	Display radix
Address	HEX
Data	HEX
Mnemonics	NONE - Disassembly generated text
Control	SYM
TXCLAV	BIN
Parity	BIN
L2PControl	SYM

If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–3.

Clocking

Clocking Options

The TMS822 support offers a bus-specific clocking mode for the TMS822 UTOPIA2 bus interface. This clocking mode is the default selection whenever you load the UTOPIA2 support.

Disassembly is not correct when using the Internal or External clocking modes. Information on basic operations in the logic analyzer online help describes how to use these clock selections for general purpose analysis.

Custom Clocking

A special clocking program is loaded on the module every time you load the UTOPIA2 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple channel groups at different times when the signals are valid on the Utopia2 bus. The module then sends all the logged in signals to the trigger machine and to the acquisition memory of the module for storage.

In the custom mode, the support uses a TxClk as the clock for the transmit interface and a RxClk as the clock for the receive interface. After loading the UTOPIA2TX or UTOPIA2RX support, the sample points and master points are defined based on the selections of each of the clocking options.

The TMS822 modifies the Custom Clocking Options menu of the logic analyzer. The following options are available to acquire Utopia2 Receive (in UTOPIA2RX) and Utopia2 Transmit (in UTOPIA2TX) bus signals:

Capture.

All Cycles (default)

Use the All Cycles option to acquire the information on the bus at every rising edge of the clock. The All Cycles option describes the conditions that exist on the bus, in addition to acquiring the ATM cells/PPP packets (in case of L2p interface) information.

ATM Cells/PPP Packets

If you choose the ATM Cells/PPP Packets option when the Utopia Level 2 interface is connected, the acquisition will consist of ATM cells only. The support does not acquire samples corresponding to cycles when valid data is not available on the interface. If you select the ATM Cells/PPP Packets option with connections to the Utopia L2p interface, the PPP packets are acquired. With the Utopia Level 2 interface, samples corresponding to cycles when valid data is not available on the interface are not acquired.

ATM Cell Headers (5-bytes)

Select the ATM Cell Headers option if only ordinary ATM cell headers must be acquired. If you select the ATM Cell Headers (5-bytes) option at the Utopia L2p interface, then the support acquires truncated PPP packets. Use the ATM Cell Headers (5-bytes) option only with the Utopia Level 2 Interface.

Polling Cycles

Select the Polling Cycles option only for multi-physical operation with polling. Selecting the Polling Cycles option helps in acquiring samples when the ATM layer device polls the PHY layer devices to determine whether they are ready to transmit or receive data. Acquisition of these cycles begins when valid data is not available on the data bus.

NOTE. *Choose this option only when the Number of PHY Ports is set to MULPHY-POLLING or MULPHY-DSI.*

Data Path Width. Use the Data Path Width option to distinguish the width of the data path. The data path width information is important when you acquire only headers. The data path width can be any one of the following:

16-bit (default)
8-bit

Number of PHY Ports. Select the number of PHY ports from one of the available selections.

SIGPHY (for SIG-PHY operation) (default)
MULPHY-DSI (for MULPHY operation with Direct Status Indication)
MULPHY-POLLING (for MULPHY operation with one TxClav and one RxClav signal)

***NOTE**. To acquire correct information, set the Data Path Width and the Number of PHY Ports appropriately.*

Utopia L2p interface supports only 16-bit data width and operates only in Multi PHY interface. Hence, Data Path Width should not be set to 8-bit and Number of PHY Ports should not be set to SIGPHY when used with L2p interface.

Extended Header Bytes are only acquired when the Custom Clocking Option Capture is set to'All Cycles' or 'ATM Cells/PPP Packets'.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The following information covers these topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Viewing cycle type labels
- Changing the way data is displayed

Acquiring Data

The TMS822 UTOPIA2 software package installs two different supports, one for the Transmit Interface, and the other for the Receive Interface.

Once you load either Transmit or Receive Interface, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations manual.

Signal Acquisition

Signal Acquisition in Transmit Mode

This section shows a timing diagram and tables that list details about how to acquire the relevant address, data, and control signals in Transmit mode.

Figure 2–1 shows a Tx bus mode timing diagram.

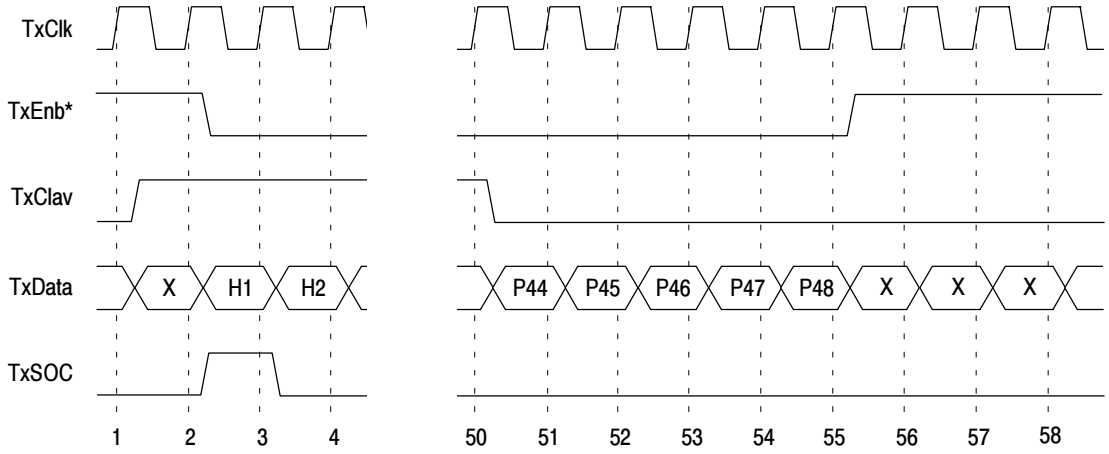


Figure 2–1: Tx bus mode timing diagram

The custom Clock uses the rising edge of the TxClk signal. Table 2–3 shows the sample points in the Transmit mode.

Table 2–3: Sample points in Tx mode

Sample points	Signals
Master Sample Point, M	All signals are mastered at the rising edge of TxClk
Sample Point, A	TxAddr4, TxAddr3, TxAddr2, TxAddr1, TxAddr0

The support provides the following options to acquire the Utopia2 Transmit bus signals.

Capture.

- All Cycles

Select the All Cycles option to acquire the information on the bus at every rising edge of the clock. This describes the conditions that exist on the bus in addition to acquiring the ATM cells/PPP Packets (in case of L2p interface) information.

The support logs in the address and masters all signals with every rising edge of the clock.

- ATM Cells/PPP Packets

Select the ATM Cells/PPP Packets option at the Utopia Level 2 interface to acquire ATM cells only. The support does not acquire samples corresponding to cycles when valid data is not available on the interface. If you select the ATM Cells/PPP Packets option with connections for Utopia L2p interface, PPP packets are acquired. In this case also, the support does not acquire samples for cycles when valid data is not available on the interface. Table 2–4 shows the signals that are acquired in the ATM Cells/PPP Packets option with reference to Figure 2–1. An asterisk (*) indicates an active low signal.

Table 2–4: Signals in the ATM Cell/PPP Packets option

Qualifiers	Operation	Signals	Position
TxEnb* high	Sample A	TxAddr4, TxAddr3, TxAddr2, TxAddr1, TxAddr0	1
TxEnb* low	Master all signals	All signals are mastered	3 through 55

- ATM Cell Headers (5-bytes)

Select the ATM Cell Headers option only if ordinary ATM cell headers must be acquired. If you select the ATM Cell Headers (5-bytes) option at the Utopia L2p interface, then the support acquires truncated PPP packets. Table 2–5 gives the signals that are acquired in the ATM Cell Headers option with reference to Figure 2–1. An asterisk (*) indicates an active low signal.

Table 2–5: Signals in the ATM Cell Headers option

Qualifiers	Operation	Signals	Position
TxEnb* low and TxSOC high	Master	All signals are mastered	3
TxEnb* high	Sample A	TxAddr4, TxAddr3, TxAddr2, TxAddr1, TxAddr0 signals are logged in	1
TxEnb* low	Master	All signals are mastered	4 through 55

- Polling Cycles

Select the Polling Cycles option only for multi-physical operation with polling. The Polling Cycles option helps to acquire samples when the ATM layer device polls the PHY layer devices to determine whether they are ready to transmit or receive data. Acquisition of these cycles begins when valid data is not available

on the data bus. Figure 2–2 shows the polling and selection phase in the transmit mode. An asterisk (*) indicates an active low signal.

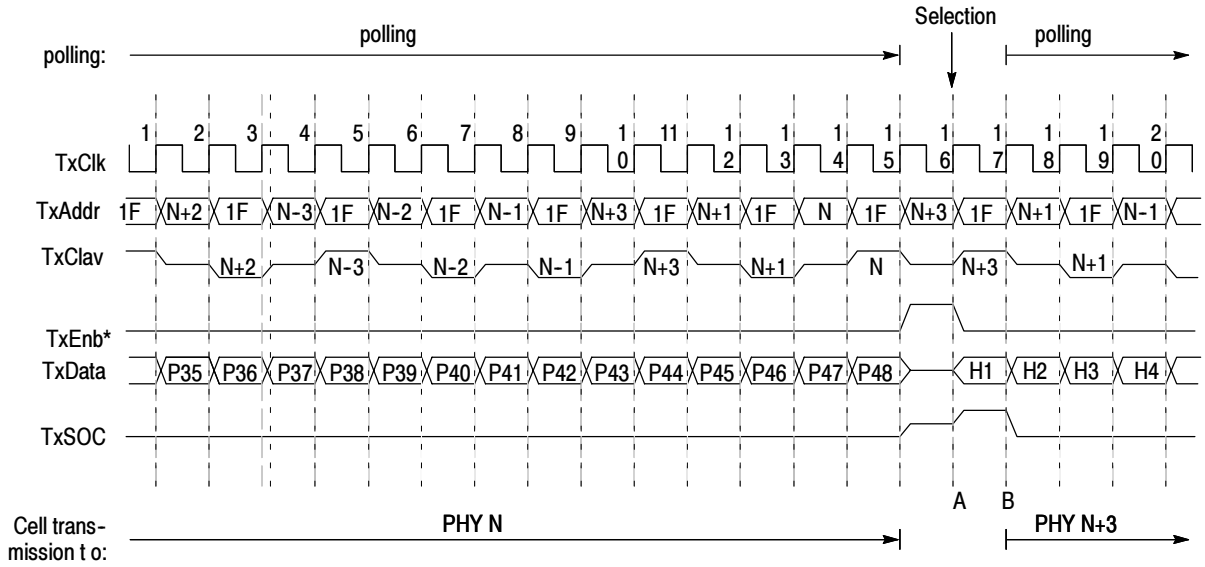


Figure 2–2: Polling and selection phase at Transmit interface

When TxEnb* high Sample Point A (Position A in Figure 2–2) is logged in, all signals are mastered at the next rising edge of TxClk (Position B in Figure 2–2).

Signal Acquisition in Receive Mode

This section shows the timing diagram and the tables that list details about acquiring the relevant address, data, and control signals in Receive mode.

Figure 2–3 shows the handshaking between the PHY and the ATM layer in Single physical mode.

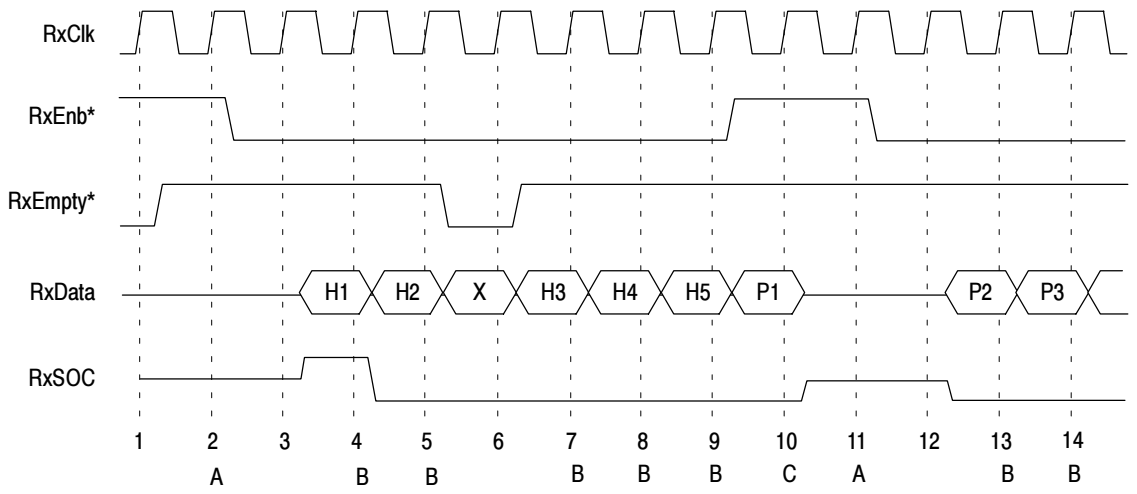


Figure 2–3: Handshaking between the PHY and ATM layer in Single physical mode

Figure 2–4 shows the handshaking between the PHY and the ATM layer in Multi physical mode. The dashed lines indicate continuation.

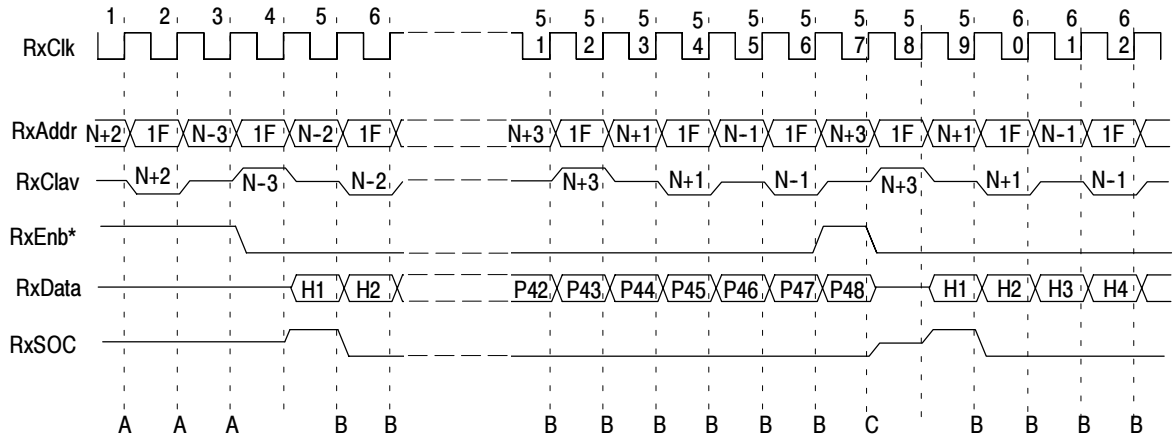


Figure 2–4: Handshaking between the PHY and ATM layer in Multi physical mode

The custom clock uses the rising edge of RxClk.

Delayed Signal. RxEnb* signal is delayed by one clock cycle.

Table 2–6 shows the sample points in the receive mode.

Table 2–6: Sample points in Rx mode

Sample point	Signals
Master Sample Point, M	All signals are mastered at the rising edge of RxClk
Sample Point, A	RxAddr4, RxAddr3, RxAddr2, RxAddr1, RxAddr0

The support provides the following options to acquire the Utopia2 Receive bus signals.

Capture.

- All Cycles

Select the All Cycles option to acquire the information on the bus at every rising edge of the clock. This describes the conditions that exist on the bus in addition to acquiring the ATM Cells/PPP Packets (for L2p interface) information.

With every rising edge of the clock, all signals are logged in and mastered.

- ATM Cells/PPP Packets

ATM Cells/PPP Packets acquisition consists of ATM cells only. Samples for cycles when valid data is not available on the interface are not acquired. If you select the ATM Cells/PPP Packets option with connections to the Utopia L2p interface, the PPP Packets are acquired. In this case also, samples for cycles when valid data is not available on the interface are not acquired.

Table 2–7 shows how signals are acquired in single physical mode with reference to Figure 2–3. An asterisk (*) indicates an active low signal.

Table 2–7: Single physical mode

Qualifiers	Operation	Signals	Position
RxEnb* High	Sample A	RxAddr4, RxAddr3, RxAddr2, RxAddr1, RxAddr0	A
RxEnb* Low and RxClav High	Master all signals	All signals are mastered	B
RxEnb* High and RxClav High	Master all signals	All signals are mastered	C

Table 2–8 shows how signals are acquired in multi physical mode with reference to Figure 2–4. An asterisk (*) indicates an active low signal.

Table 2–8: Multi physical mode

Qualifiers	Operation	Signals	Position
RxEnb* High	Sample A	RxAddr4, RxAddr3, RxAddr2, RxAddr1, RxAddr0	A
RxEnb* Low	Master all signals	All signals are mastered	B
RxEnb* High	Sample A and Master all signals	RxAddr4, RxAddr3, RxAddr2, RxAddr1, RxAddr0 and all other signals are mastered	C

- ATM Cell Headers (5-bytes)

Select the ATM Cell Headers option only if ordinary ATM cell headers must be acquired. If you select the ATM Cell Headers (5-bytes) option at Utopia L2p interface, then the support acquires truncated PPP packets.

- Polling Cycles

Select the Polling Cycles option only for multi-physical operation with polling. The Polling Cycles option helps in acquiring samples when the ATM layer device polls the PHY layer devices to determine whether they are ready to transmit or receive data. Acquisition of these cycles begins when valid data is not available on the data bus. If you select Polling Cycles for single physical mode, there is no meaning to the acquired information.

Figure 2–5 shows the polling and selection phase at the Receive interface.

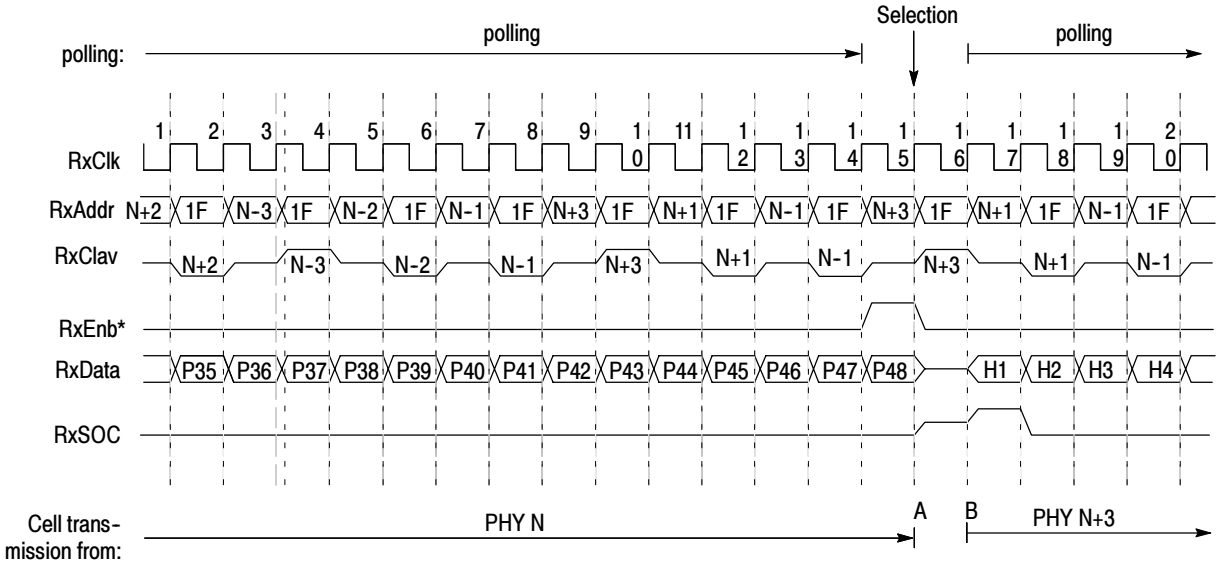


Figure 2–5: Polling and selection phase at Receive interface

When RxEnb* high Sample Point A (Position A in the Figure 2–5) is logged in and at the next rising edge of RxClk, all signals are mastered (Position B in the Figure 2–5).

Viewing Disassembled Data

You can view disassembled data in six display formats:

All Utopia Cycles (Disassembly)
All UtopiaL2p Cycles (Disassembly)
ATM Cells (Disassembly)
PPP Packets (Disassembly)
ATM Cell Headers (Disassembly)
Polling Cycles (Disassembly)

The information on basic operations describes how to select the disassembly display formats.

***NOTE**. You must set the selections in the Disassembly property page (the Disassembly Format Definition overlay) correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–22.*

For the UTOPIA2 support, the default display format shows the Address and Data channel group values for each sample of acquired data.

If a channel group is not visible, you must use Add Column or Ctrl+L to make the group visible.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2-9 shows these special characters and strings and describes what they represent.

Table 2-9: Description of special characters in the display

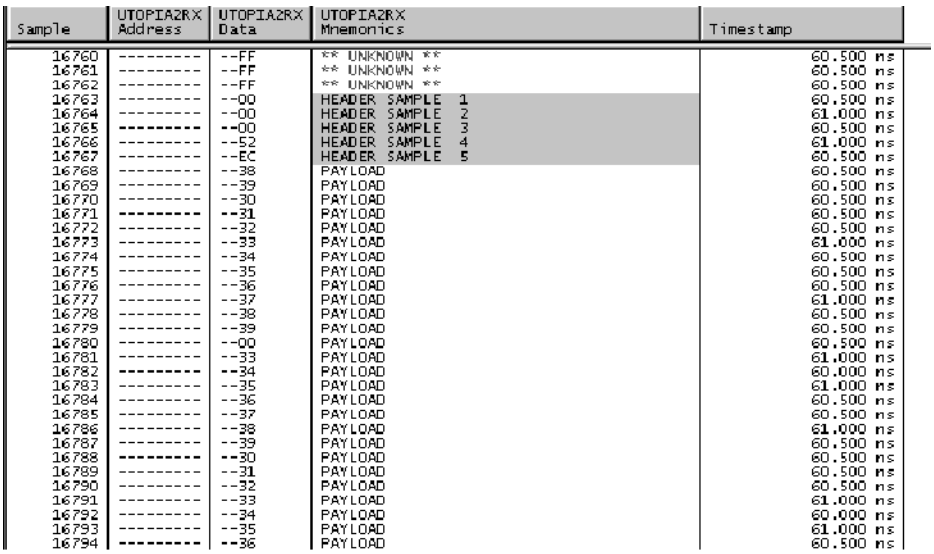
Character or string displayed	Description
0x	Indicates that the given number is in hexadecimal.
>	Insufficient room on the screen to show all available data.
t	Indicates that the given number is in decimal.
0b	Indicates that the given number is in binary.

***NOTE**. The display options All Utopia Cycles, ATM Cells, ATM Cell Headers, and Polling Cycles are used with UTOPIA Level 2 Interface. The display options All UtopiaL2p Cycles, and PPP Packets are used with UTOPIA Level 2 Plus Interface.*

All Utopia Cycles Display Format

Along with the 'All Cycles' option in custom clocking, the All Utopia Cycles Display Format provides disassembly of all the cycles including those where valid data transfers are not available. The All Utopia Cycles Display Format displays all the valid ATM cell headers and their payloads, any Invalid cycles, and Polling cycles that occur.

Figure 2–6 shows an example of the All Utopia Cycles display format.



Sample	UTOPIA2RX Address	UTOPIA2RX Data	UTOPIA2RX Mnemonics	Timestamp
16760	---------	--FF	** UNKNOWN **	60.500 ns
16761	---------	--FF	** UNKNOWN **	60.500 ns
16762	---------	--FF	** UNKNOWN **	60.500 ns
16763	---------	--00	HEADER SAMPLE 1	60.500 ns
16764	---------	--00	HEADER SAMPLE 2	61.000 ns
16765	---------	--00	HEADER SAMPLE 3	60.500 ns
16766	---------	--52	HEADER SAMPLE 4	61.000 ns
16767	---------	--EC	HEADER SAMPLE 5	60.500 ns
16768	---------	--38	PAYLOAD	60.500 ns
16769	---------	--39	PAYLOAD	60.500 ns
16770	---------	--30	PAYLOAD	60.500 ns
16771	---------	--31	PAYLOAD	60.500 ns
16772	---------	--32	PAYLOAD	60.500 ns
16773	---------	--33	PAYLOAD	61.000 ns
16774	---------	--34	PAYLOAD	60.500 ns
16775	---------	--35	PAYLOAD	60.500 ns
16776	---------	--36	PAYLOAD	60.500 ns
16777	---------	--37	PAYLOAD	61.000 ns
16778	---------	--38	PAYLOAD	60.500 ns
16779	---------	--39	PAYLOAD	60.500 ns
16780	---------	--00	PAYLOAD	60.500 ns
16781	---------	--33	PAYLOAD	61.000 ns
16782	---------	--34	PAYLOAD	60.000 ns
16783	---------	--35	PAYLOAD	61.000 ns
16784	---------	--36	PAYLOAD	60.500 ns
16785	---------	--37	PAYLOAD	60.500 ns
16786	---------	--38	PAYLOAD	61.000 ns
16787	---------	--39	PAYLOAD	60.500 ns
16788	---------	--30	PAYLOAD	60.500 ns
16789	---------	--31	PAYLOAD	60.500 ns
16790	---------	--32	PAYLOAD	60.500 ns
16791	---------	--33	PAYLOAD	61.000 ns
16792	---------	--34	PAYLOAD	60.000 ns
16793	---------	--35	PAYLOAD	61.000 ns
16794	---------	--36	PAYLOAD	60.500 ns

Figure 2–6: Example of All Utopia Cycles display format

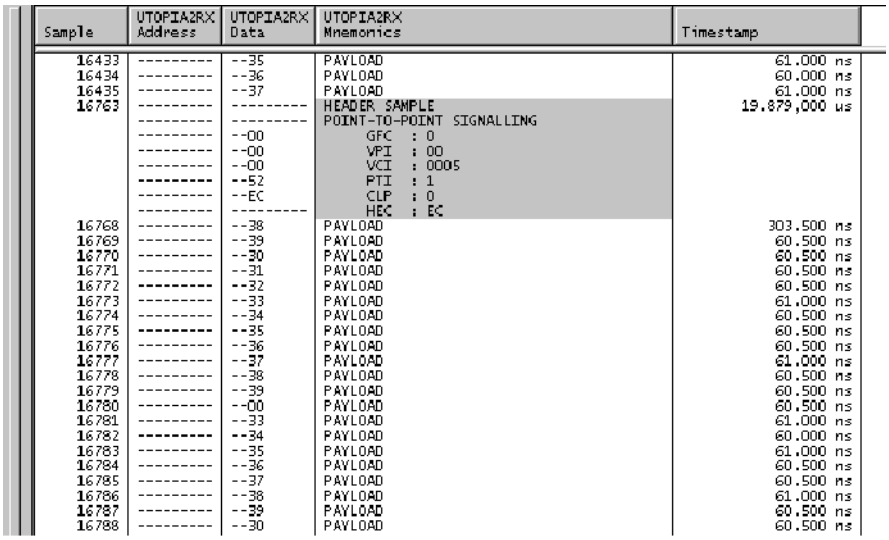
All UtopiaL2p Cycles Display Format

Along with the ‘All Cycles’ option in custom clocking, the All UtopiaL2p Cycles Display Format provides disassembly of all L2p cycles including those where valid data transfers are not available. The All UtopiaL2p Cycles Display Format displays PPP Packets, Filler Data and any Invalid cycles.

ATM Cells Display Format

Along with the ‘All Cycles’ or ‘ATM Cells/PPP Packets’ option in custom clocking, the ATM Cells Display Format shows the header details and payload information. In addition, if you select the AAL type, then payload is further disassembled to show details of AAL SAR-PDU. Along with the ‘ATM Cell Headers’ option in custom clocking, the ATM Cells Display Format shows only the ATM cell header details.

Figure 2–7 shows an example of the ATM Cells display format.



Sample	UTOPIA2RX Address	UTOPIA2RX Data	UTOPIA2RX Mnemonics	Timestamp
16433	---------	--35	PAYLOAD	61.000 ns
16434	---------	--36	PAYLOAD	60.000 ns
16435	---------	--37	PAYLOAD	61.000 ns
16763	---------	---------	HEADER SAMPLE	19.879,000 us
	---------	---------	POINT-TO-POINT SIGNALLING	
	---------	--00	GFC : 0	
	---------	--00	VPI : 00	
	---------	--00	VCI : 0005	
	---------	--52	PTI : 1	
	---------	--EC	CLP : 0	
	---------	---------	HEC : EC	
16768	---------	--38	PAYLOAD	303.500 ns
16769	---------	--39	PAYLOAD	60.500 ns
16770	---------	--30	PAYLOAD	60.500 ns
16771	---------	--31	PAYLOAD	60.500 ns
16772	---------	--32	PAYLOAD	60.500 ns
16773	---------	--33	PAYLOAD	61.000 ns
16774	---------	--34	PAYLOAD	60.500 ns
16775	---------	--35	PAYLOAD	60.500 ns
16776	---------	--36	PAYLOAD	60.500 ns
16777	---------	--37	PAYLOAD	61.000 ns
16778	---------	--38	PAYLOAD	60.500 ns
16779	---------	--39	PAYLOAD	60.500 ns
16780	---------	--00	PAYLOAD	60.500 ns
16781	---------	--33	PAYLOAD	61.000 ns
16782	---------	--34	PAYLOAD	60.000 ns
16783	---------	--35	PAYLOAD	61.000 ns
16784	---------	--36	PAYLOAD	60.500 ns
16785	---------	--37	PAYLOAD	60.500 ns
16786	---------	--38	PAYLOAD	61.000 ns
16787	---------	--39	PAYLOAD	60.500 ns
16788	---------	--30	PAYLOAD	60.500 ns

Figure 2–7: Example of ATM Cells display format

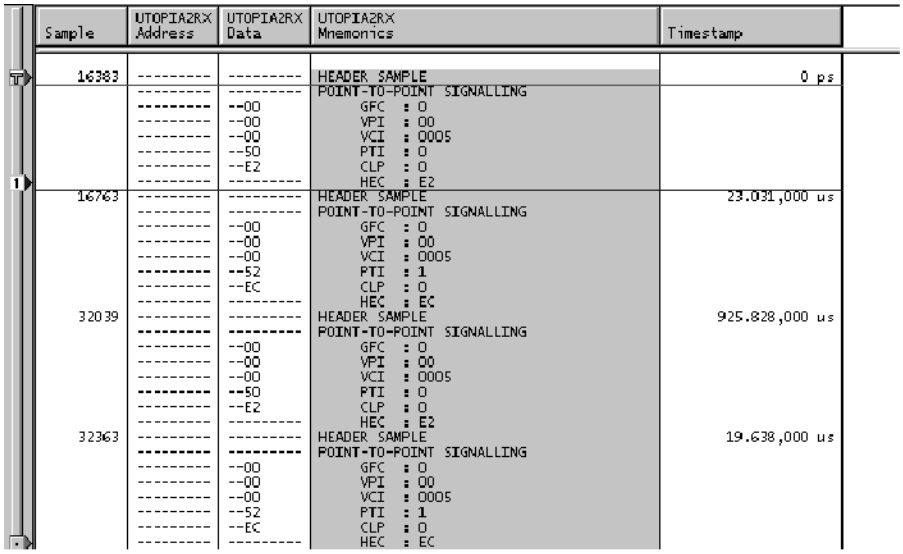
PPP Packets Display Format

Along with the ‘All Cycles’ or ‘ATM Cells/PPP Packets’ option in custom clocking, the PPP Packets Display Format shows acquired PPP packets. The PPP packets are not decoded to show PPP information.

ATM Cell Headers Display Format

Along with the ‘All Cycles’, ‘ATM Cells/PPP Packets’ or ‘ATM Cell Headers (5-bytes)’ option in custom clocking, the ATM Cell Headers Display Format displays only the header details.

Figure 2–8 shows an example of the ATM Cell Headers display format.



Sample	UTOPIA2RX Address	UTOPIA2RX Data	UTOPIA2RX Mnemonics	Timestamp
16383	---------	---------	HEADER SAMPLE	0 ps
	---------	---------	POINT-TO-POINT SIGNALLING	
	---------	--00	GFC : 0	
	---------	--00	VPI : 00	
	---------	--00	VCI : 0005	
	---------	--50	PTI : 0	
	---------	--E2	CLP : 0	
	---------	---------	HEC : E2	
16763	---------	---------	HEADER SAMPLE	23.031,000 us
	---------	---------	POINT-TO-POINT SIGNALLING	
	---------	--00	GFC : 0	
	---------	--00	VPI : 00	
	---------	--00	VCI : 0005	
	---------	--52	PTI : 1	
	---------	--EC	CLP : 0	
	---------	---------	HEC : EC	
32039	---------	---------	HEADER SAMPLE	925.828,000 us
	---------	---------	POINT-TO-POINT SIGNALLING	
	---------	--00	GFC : 0	
	---------	--00	VPI : 00	
	---------	--00	VCI : 0005	
	---------	--50	PTI : 0	
	---------	--E2	CLP : 0	
	---------	---------	HEC : E2	
32363	---------	---------	HEADER SAMPLE	19.638,000 us
	---------	---------	POINT-TO-POINT SIGNALLING	
	---------	--00	GFC : 0	
	---------	--00	VPI : 00	
	---------	--00	VCI : 0005	
	---------	--52	PTI : 1	
	---------	--EC	CLP : 0	
	---------	---------	HEC : EC	

Figure 2–8: Example of ATM Cell Headers display format

Polling Cycles Display Format

Select the Polling Cycles Display Format option in the disassembly to display only polling cycles. The Polling Cycles option is valid only for MULPHY operations.

***NOTE**. For correct disassembly, follow these steps:*

When MULPHY operates with one TxClav and one RxClav, the Number of PHY Ports should be set to MULPHY-POLLING in both clocking and disassembly. Set the clocking option Capture to Polling Cycles.

When MULPHY operates with Direct Status Indication, the Number of PHY Ports should be set to MULPHY-DSI in both clocking and disassembly. Set the clocking option Capture to Polling Cycles.

UTOPIA2 Specific Labels

This section gives information about the labels used in TMS822 UTOPIA2 support.

Table 2-10: UTOPIA2 specific labels

UTOPIA2 specific label (Mnemonics)	Definition
HEADER SAMPLE *Byte Number*	Header byte of the Atm Cell. Byte Number refers to the corresponding header byte. For example: HEADER SAMPLE 1 refers to first header byte of the cell.
EXTENDED HEADER SAMPLE *Byte Number*	Refers to the Extended Header Bytes. Byte Number refers to the corresponding header byte.
PAYLOAD	Refers to the ATM cell payload
*** HEADER TRUNCATED ***	Displayed when all the 5 header bytes are not available for disassembly.
*** PAYLOAD TRUNCATED ***	Displayed when all the 48 bytes of payload are not available for disassembly.
PORT 0x Address NOT READY	Displayed when the physical port is not ready for transmission or reception. Address indicates the address of the corresponding port.
PORT 0x Address READY	Displayed when the physical port is ready for transmission or reception. Address indicates the address of the corresponding port.
PACKETS	Displayed when L2p packets are identified.
FILLER DATA	Displayed when data stream from L2p interface are not occupied by frame data.
POLLING CYCLES	Displayed when polling cycles are acquired from MULPHY interface.
*** CELL TRUNCATED ***	Displayed when all bytes of ATM cell are not available for disassembly. This happens at the start and end of acquisition.
*** INVALID DATA ***	Displayed when an invalid cycle occurs.
*** UNKNOWN ***	Displayed when an unknown combination of control bits occurs.

For the following labels, refer to B-ISDN ATM layer specification ITU-T I.361.

ATM cell header details:

GFC
VPI
VCI
PTI
CLP
HEC
UDF2

The following strings are displayed corresponding to the preassigned header fields:

UNASSIGNED CELL
INVALID
META-SIGNALLING
GENERAL BROADCAST SIGNALLING
POINT-TO-POINT SIGNALLING
RESERVED FOR FUTURE FUNCTIONS
RESERVED FOR FUTURE VP FUNCTIONS
SEGMENT OAM F4 FLOW CELL
END-TO-END OAM F4 FLOW CELL
VP RESOURCE MANAGEMENT CELL
SEGMENT OAM F5 FLOW CELL
END TO END OAM F5 FLOW CELL
VC RESOURCE MANAGEMENT CELL
RESERVED FOR FUTURE VC FUNCTIONS
RESERVED FOR FUTURE FUNCTIONS
NNI SIGNALLING
NOT PRE_ASSIGNED

For the following labels, refer to B-ISDN ATM Adaptation Layer Specification ITU-T I.363.1.

AAL1:

SAR-PDU HEADER
SN
SN-CSI Bit
SN-Sequence Count Field
SNP Field
SNP-CRC Field Bit
SNP-Even Parity Bit
SAR-PDU PAYLOAD

For the following labels, refer to B-ISDN ATM Adaptation Layer Specification ITU-T I.363.2.

AAL 2:

CPS-PDU Start Field
CPS-PDU Offset Field
CPS-PDU Sequence Number
CPS-PDU Parity
CPS-PDU PAYLOAD
CPS-PDU PACKET HEADER
CPS-PDU Channel Identifier
CPS-PDU PACKET PAYLOAD
CPS-PDU Length Indicator

CPS-PDU HEC
CPS-PDU UUI

For the following labels refer to B-ISDN ATM Adaptation Layer Specification ITU-T I.363.3.

AAL3/4:

DATA-SAR-PDU HEADER
ABORT-SAR-PDU HEADER
BOM
COM
EOM
SSM
ST
SN
MID
ABORT-SAR-PDU TRAILER
DATA-SAR-PDU TRAILER
LI
CRC
CPCS-PDU HEADER
CPI
Btag
Basize
ABORT-SAR-PDU PAYLOAD
DATA-SAR-PDU PAYLOAD
CPCS-PDU TRAILER
Alignment
Etag
Length
UNUSED DATA

For the following labels refer to B-ISDN ATM Adaptation Layer Specification ITU-T I.363.5.

AAL 5:

SAR-PDU PAYLOAD
CPCS-UU
CPCS-CPI
CPCS SDU Length
CPCS-CRC

Changing How Data is Displayed

Common fields and features allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the TMS822 UTOPIA2 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

Table 2–11 shows the logic analyzer disassembly display options.

Table 2–11: Logic analyzer disassembly display options

Description	Option
Show:	All Utopia Cycles (Default) All UtopiaL2p Cycles ATM Cells PPP Packets ATM Cell Headers Polling Cycles
Disassemble Across Gaps:	Yes No (Default)

***NOTE**. The display options All Utopia Cycles, ATM Cells, ATM Cell Headers, and Polling Cycles are used with UTOPIA Level 2 Interface. The display options All UtopiaL2p Cycles, and PPP Packets are used with UTOPIA Level 2 Plus Interface.*

All Utopia Cycles. Along with the 'All Cycles' option in custom clocking, the All Utopia Cycles provides disassembly of all the cycles including those where valid data transfers are not available. The All Utopia Cycles option displays all the valid ATM cell headers and their payloads, any Invalid cycles, and Polling cycles that occur.

All Utopia L2p Cycles. Along with the 'All Cycles' option in custom clocking, the All UtopiaL2p Cycles provides disassembly of all L2p cycles including those where valid data transfers are not available. The All Utopia L2p Cycles format displays PPP Packets, Filler Data and any Invalid cycles.

ATM Cells. Along with the 'All Cycles' or 'ATM Cells/PPP Packets' option in custom clocking, the ATM Cells shows the header details and payload information. In addition, if you select the AAL type, then payload is further disassembled to show details of AAL SAR-PDU. Along with the 'ATM Cell Headers' option in custom clocking, the ATM Cells Display Format shows only the ATM cell header details.

PPP Packets. Along with the 'All Cycles' or 'ATM Cells/PPP Packets' option in custom clocking, the PPP Packets shows acquired PPP packets. The PPP packets are not decoded to show PPP information.

ATM Cell Headers. Along with the 'All Cycles', 'ATM Cells/PPP Packets' or 'ATM Cell Headers (5-bytes)' option in custom clocking, the ATM Cell Headers displays only the header details.

Polling Cycles. The Polling Cycles option displays only the polling cycles. The Polling Cycles option is available only for MULPHY operations.

***NOTE**. For correct disassembly, follow these steps:*

When MULPHY operates with one TxClav and one RxClav, the Number of PHY Ports should be set to MULPHY-POLLING in both clocking and disassembly. Set the clocking option Capture to Polling Cycles.

When MULPHY operates with Direct Status Indication, the Number of PHYPorts should be set to MULPHY-DSI in both clocking and disassembly. Set the clocking option Capture to Polling Cycles.

Bus Specific Fields

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways.

Data Path Width. You can select one of the available bit modes from the dropdown list.

Data Path Width: 16-bit (default)
8-bit

Number of PHY Ports. The Utopia Level 2 interface has three interface modes: SIGPHY, MULPHY-DSI, and MULPHY-POLLING. Select one of the following options.

SIGPHY (Default) (Single PHY interface). If you select the SIGPHY option, one ATM layer port and one PHY layer port are connected. No address information is available and a single TxClav and RxClav signal exists. SIGPHY is the default selection.

MULPHY-DSI (Multiple PHY interface Direct status indication). If you select the MULPHY-DSI option, one ATM layer port and Multiple physical layer ports are connected. The transaction on the bus includes the address information and the additional TxClav [3:1] signals. In this mode, you can connect a maximum of four physical ports to the ATM device. Each port uses a dedicated Tx/RxClav line for handshaking.

MULPHY-POLLING (Multiple PHY interface under polling). In the MULPHY-POLLING mode, only one Tx/RxClav signal exists. The physical port to which the ATM device transmits or receives is decided by polling the single Tx/RxClav signal and presenting device addresses on the address bus.

Extended Header Bytes. The ATM forum specification specifies that the ATM header field consists of 5-bytes. Many commercially available ATM systems (including that of Motorola 8260) allow you to specify up to 12 extra header bytes (tag bytes). The extended-header-bytes option provides an editable field (the default value is 0), where you can enter the extended header length in hexadecimal. The extra header bytes are displayed and their meanings are not decoded since their interpretation can vary from user to user.

Type of Interface. You can select the type of interface by selecting one of the two available options.

UNI (Default): Select the UNI option to display the header fields including the Generic Flow Control (GFC). The VPI field width is 8 bits, the VCI field width is 16 bits, PTI field width is 3 bits, and CLP field width is 1 bit.

NNI: Select the NNI option to display the header fields (does not include GFC). The subsequent field, VPI, is 12 bits in length instead of 8 bits as in UNI.

Type of AAL. Select the Type of AAL option to indicate how the payload information must be interpreted. The format of the SAR-PDUs displayed depends on this option. Select the AAL type from the available options.

AAL 0 (default)
AAL 1
AAL 2
AAL 3/4
AAL 5

Trigger Programs

This section describes how to install and load trigger programs. A trigger library containing programs that can trigger on preassigned header field combinations is provided on your disk. The preassigned header field combinations are restricted to the combinations mentioned in the ITU-T recommendation I.361.

Installing Trigger Programs

The trigger programs are installed along with the TMS822 UTOPIA2 support package:

- Trigger Programs for the Transmit Interface are in C:\Program Files\TLA 700\ Supports\UTOPIA2TX folder.
- Trigger Programs for the Receive Interface are in C:\Program Files\TLA 700\ Supports\UTOPIA2RX folder.

Loading Trigger Programs

To load a trigger program from UTOPIA2TX or UTOPIA2RX support, follow these steps:

1. Load the support package.
2. From the system window, click the 

Trigger button.
3. From the Trigger window, click the  Load Trigger Toolbar button.
4. From the Load LA Trigger dialog box, click the Browse button. Figure 2–9 shows the Load LA Trigger screen.

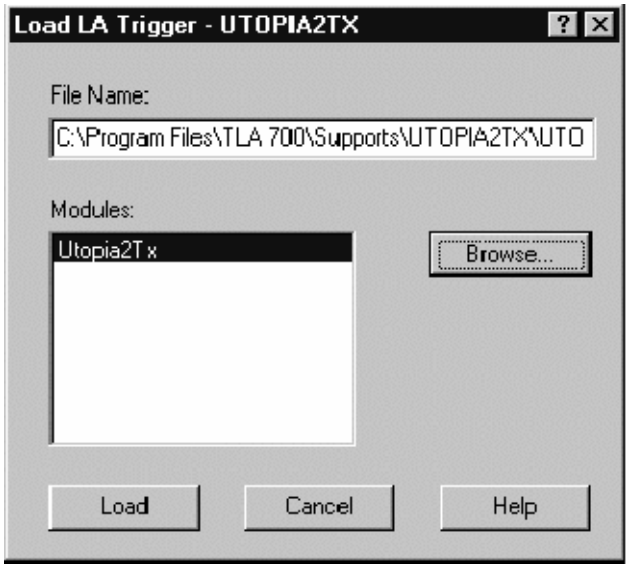


Figure 2-9: Loading trigger programs

Select the Transmit Trigger Programs from the path C:\Program Files\TLA 700\ Supports\UTOPIA2TX.

Select the Receive Trigger Programs from the path C:\Program Files\TLA 700\ Supports\UTOPIA2RX.

5. Select a trigger program from the list.
6. Click Open to apply the selection.
7. Click Load to load the trigger program into the module.

For more information, refer to the logic analyzer online help and the logic analyzer user manual.

The trigger programs follow these conventions:

Bits with the lowest numbers are treated as LSB bits and bits with the highest numbers are treated as MSB bits.

For example: D15.....D0
(MSB) (LSB)

File Name Conventions for Transmit Interface. Trigger programs have the following file naming conventions.

UTOPIA2TX(For Transmit Interface): UTOPIA2TX_TrigOn_DataWidth_InterfaceType_Pre-assigned Cell Type.tla,

where,

DataWidth:
16-bit: Logic analyzer file names with the 16-bit suffix are the trigger programs to be used when the data path width is 16-bit.

8-bit: Logic analyzer file names with the 8-bit suffix are the trigger programs to be used when the data path width is 8-bit.

InterfaceType:
UNI: Logic analyzer file names with the UNI suffix are the trigger programs to be used when the interface is 'User Network Interface'.

NNI: Logic analyzer file names with the NNI suffix are the trigger programs to be used when the interface is 'Network Node Interface'.

Preassigned Cell Type: These are the various cell types based on the preassigned header field combinations as mentioned in the ITU-T Recommendation I.361. The cell types have preassigned combinations of VPI, VCI, PTI and CLP values at UNI (User Network Interface) and NNI (Network Node Interface).

File Name Conventions for Receive Interface. Trigger programs have the following file naming conventions.

UTOPIA2RX_TrigOn_DataWidth_InterfaceType_No of PHYports_Pre-assigned Cell Type.tla

where,

DataWidth:
16-bit: Logic analyzer file names with the 16-bit suffix are the trigger programs to be used when the data path width is 16-bit.

8-bit: Logic analyzer file names with the 8-bit suffix are the trigger programs to be used when the data path width is 8-bit.

Interface Type:
UNI: Logic analyzer file names with the UNI suffix are the trigger programs to be used when the interface is 'User Network Interface'.

NNI: Logic analyzer file names with the NNI suffix are the trigger programs to be used when the interface is 'Network Node Interface'.

No of PHY Ports:
SIGPHY: Logic analyzer file names with the SIGPHY suffix are the trigger programs to be used when the interface is Single Physical. For example, in the SIGPHY configuration one ATM layer port and one PHY layer port are connected.

MULPHY: Logic analyzer file names with the MULPHY suffix are the trigger programs to be used when the interface is Multi Physical. For example, in the Multi Physical configuration, one ATM layer port and more than one PHY layer ports are connected.

Preassigned Cell Type: These are the various cell types based on the preassigned header field combinations as mentioned in the ITU-T Recommendation I.361. The cell types have preassigned combinations of VPI, VCI, PTI and CLP values at UNI (User Network Interface) and NNI (Network Node Interface).

***NOTE**. Do not edit the trigger programs provided with the support.*

Reference

Symbol and Channel Assignment Tables

This section lists the symbol tables and channel assignment tables for disassembly and timing.

Symbol Tables

The TMS822 support supplies four symbol table files.

- Control Group Symbol Tables for UTOPIA2 Transmit and Receive Interface
- L2PControl Group Symbol Tables for UTOPIA L2p Transmit and Receive Interface

The UTOPIA2RX_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group in UTOPIA2 Receive support. The UTOPIA2TX_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group in UTOPIA2 Transmit support. This also applies to other symbol tables.

Symbol tables are generally not for use in timing or UTOPIA2 support disassembly.

Tables 3–1 through 3–4 show the definitions for name, bit pattern, and meaning of the group symbols in Control file, and L2PControl groups for Utopia Transmit and Receive interface support.

Table 3-1: UTOPIA2RX_Ctrl group symbol table definitions

Symbol	Control group value RxEmpty*/RxClav RxSOC RxEnb*	Description
Rx_in_progress	X 0 0	Reception in progress
Start_of_Cell	X 1 0	Start of Header
ATM/PHY_NotRdy	X 1 1	ATM or PHY is not ready

Table 3-2: UTOPIA2TX_Ctrl group symbol table definitions

Symbol	Control group value TxFull*/TxClav TxSOC TxEnb*	Description
Tx_in_progress	X 0 0	Transmission in progress
Start_of_Cell	X 1 0	Start of Cell
ATM/PHY_NotRdy	X X 1	ATM or PHY is not ready

Table 3-3: UTOPIA2RX_L2pctrl group symbol table definitions

Symbol	Receive L2PControl group value RXEOFO RXSOFO RXABTO RXMSO RXFCSEO	Description
FCS_ERROR:CYCLE_ABORTED	1 0 X 1 1	FCS Error and Cycle Aborted
CYCLE_ABORTED	1 0 1 1 X	Cycle aborted
FCS_ERROR	1 0 X X 1	FCS Error
EOF:MSB_VALID	1 0 X 1 0	End of Frame - in MSB of current word
EOF	1 0 X 0 0	End of Frame - in LSB of current word
FRAME_START	0 1 X X X	Start of Frame

Table 3-4: UTOPIA2TX_L2pctrl group symbol table definitions

Symbol	Transmit L2PControl group value TXEOFI TXSOFI TXABTO TXMSI	Description
EOF:MSB_VALID	1 0 X 1	End of Frame - LastByte of frame in MSB position of 16 bit word
EOF	1 0 X 0	End of Frame - LastByte of frame in LSB position of 16 bit word
FRAME_START	0 1 X X	Start of Frame

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as for the Address channel group.

Channel Assignment Tables

Channel assignments shown in Table 3–5 through Table 3–16 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules, unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

Channel Assignment for Utopia2 Receive Interface

Table 3–5 shows the probe section and channel assignments for the logic analyzer Address group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-5: Address group channel assignments for UTOPIA2RX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor C pin 13	C3:4 (MSB)	RxAddr4
Mictor C pin 15	C3:3	RxAddr3
Mictor C pin 17	C3:2	RxAddr2
Mictor C pin 19	C3:1	RxAddr1
Mictor C pin 21	C3:0 (LSB)	RxAddr0

Table 3–6 shows the probe section and channel assignments for the Data group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-6: Data group channel assignments for UTOPIA2RX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor A pin 07	A3:7 (MSB)	RxData15
Mictor A pin 09	A3:6	RxData14

Table 3-6: Data group channel assignments for UTOPIA2RX signals (cont.)

AMP mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor A pin 11	A3:5	RxData13
Mictor A pin 13	A3:4	RxData12
Mictor A pin 15	A3:3	RxData11
Mictor A pin 17	A3:2	RxData10
Mictor A pin 19	A3:1	RxData9
Mictor A pin 21	A3:0	RxData8
Mictor A pin 23	A2:7	RxData7
Mictor A pin 25	A2:6	RxData6
Mictor A pin 27	A2:5	RxData5
Mictor A pin 29	A2:4	RxData4
Mictor A pin 31	A2:3	RxData3
Mictor A pin 33	A2:2	RxData2
Mictor A pin 35	A2:1	RxData1
Mictor A pin 37	A2:0 (LSB)	RxData0

Table 3–7 shows the probe section and channel assignments for the Control group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is UTOPIA2RX_Ctrl

Table 3-7: Control group channel assignments for UTOPIA2RX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor C pin 33	C2:2 (MSB)	RxEmpty*/RxClav
Mictor C pin 35	C2:1	RxSOC
Mictor C pin 37	C2:0 (LSB)	RxEnb*

Table 3–8 shows the probe section and channel assignments for the RXCLAV (Cell Available) group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-8: RXCLAV group channel assignments for UTOPIA2RX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor C pin 27	C2:5 (MSB)	RxClav3
Mictor C pin 29	C2:4	RxClav2
Mictor C pin 31	C2:3	RxClav1
Mictor C pin 33	C2:2 (LSB)	RxEmpty*/RxClav

Table 3–9 shows the probe section and channel assignments for the Parity group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-9: Parity group channel assignments for UTOPIA2RX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor C pin 25	C2:6	RxPrty

Table 3–10 shows the probe section and channel assignments for the L2PControl group and the bus signal to which each channel connects. By default, this channel group is displayed as symbols. The symbol table file name is UTOPIA2RX_L2pctrl on the logic analyzer.

Table 3-10: L2PControl group channel assignments for UTOPIA2RX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor C pin 11	C3:5 (MSB)	RXEOFO
Mictor C pin 09	C3:6	RXSOFO
Mictor C pin 23	C2:7	RXABTO
Mictor C pin 07	C3:7	RXMSO
Mictor A pin 05	CLK:0 (LSB)	RXFCSEO

Channel Assignments for Utopia2 Transmit Interface

Table 3–11 shows the probe section and channel assignments for the Address group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-11: Address group channel assignments for UTOPIA2TX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor C pin 13	C3:4 (MSB)	TxAddr4
Mictor C pin 15	C3:3	TxAddr3
Mictor C pin 17	C3:2	TxAddr2
Mictor C pin 19	C3:1	TxAddr1
Mictor C pin 21	C3:0 (LSB)	TxAddr0

Table 3–12 shows the probe section and channel assignments for the Data group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-12: Data group channel assignments for UTOPIA2TX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor A pin 07	A3:7 (MSB)	TxData15
Mictor A pin 09	A3:6	TxData14
Mictor A pin 11	A3:5	TxData13
Mictor A pin 13	A3:4	TxData12
Mictor A pin 15	A3:3	TxData11
Mictor A pin 17	A3:2	TxData10
Mictor A pin 19	A3:1	TxData9
Mictor A pin 21	A3:0	TxData8
Mictor A pin 23	A2:7	TxData7
Mictor A pin 25	A2:6	TxData6
Mictor A pin 27	A2:5	TxData5
Mictor A pin 29	A2:4	TxData4
Mictor A pin 31	A2:3	TxData3
Mictor A pin 33	A2:2	TxData2

Table 3-12: Data group channel assignments for UTOPIA2TX signals (cont.)

AMP mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor A pin 35	A2:1	TxData1
Mictor A pin 37	A2:0 (LSB)	TxData0

Table 3–13 shows the probe section and channel assignments for the logic analyzer Control group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is UTOPIA2TX_Ctrl on the logic analyzer.

Table 3-13: Control group channel assignments for UTOPIA2TX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor C pin 33	C2:2 (MSB)	TxFull*/TxClav
Mictor C pin 35	C2:1	TxSOC
Mictor C pin 37	C2:0 (LSB)	TxEnb*

Table 3–14 shows the probe section and channel assignments for the TXCLAV group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-14: TXCLAV group channel assignments for UTOPIA2TX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor C pin 27	C2:5 (MSB)	TxClav3
Mictor C pin 29	C2:4	TxClav2
Mictor C pin 31	C2:3	TxClav1
Mictor C pin 33	C2:2 (LSB)	TxFull*/TxClav

Table 3–15 shows the probe section and channel assignments for the logic analyzer Parity group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-15: Parity group channel assignments for UTOPIA2TX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor C pin 25	C2:6	TxPrty

Table 3–16 shows the probe section and channel assignments for the logic analyzer L2PControl group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is UTOPIA2TX_L2pctrl on the logic analyzer.

Table 3-16: L2PControl group channel assignments for UTOPIA2TX signals

AMP mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor C pin 11	C3:5 (MSB)	TXEOFI
Mictor C pin 09	C3:6	TXSOFI
Mictor C pin 23	C2:7	TXABTO
Mictor C pin 07	C3:7 (LSB)	TXMSI

Logic Analyzer Channels not Connected

Extra channels that are not connected in the TMS822 UTOPIA2 support are:

Clk0 in Transmit Mode (UTOPIA2TX support)

Clock and Qualifier Channels

Table 3–17 and Table 3–18 show the probe section and channel assignments for the clock probes (not part of any group), and the TMS822 UTOPIA2 signal to which each channel connects.

Table 3-17: Clock channel assignments for UTOPIA2RX

Logic analyzer section & probe	UTOPIA2RX signal name
Clock:3	RxClk

Table 3-18: Clock channel assignments for UTOPIA2TX

Logic analyzer section & probe	UTOPIA2TX signal name
Clock:3	TxClk

Tables 3–19 through 3–20 list the qualifier channel assignments for the Utopia2 Receive and Transmit interfaces.

Table 3-19: Qualifier channel assignments for UTOPIA2RX

Logic analyzer section & probe	UTOPIA2RX signal name
C2:2	RxEmpty*/RxClav
C2:1	RxSOC
C2:0	RxEnb*

Table 3-20: Qualifier channel assignments for UTOPIA2TX

Logic analyzer section & probe	UTOPIA2TX signal name
C2:2	TxFull*/TxClav
C2:1	TxSOC
C2:0	TxEnb*

Additional Signals Required for Disassembly from Utopia L2p Interface

Tables 3–21 and 3–22 show signals that are required only when the interface is Utopia Level 2 Plus interface.

Table 3-21: Signals required for Utopia Level 2 Plus Transmit interface

AMP Mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor C pin 7	C3:7	TXMSI
Mictor C pin 9	C3:6	TXSOFI
Mictor C pin 11	C3:5	TXEOFI
Mictor C pin 23	C2:7	TXABTO

Table 3-22: Signals required for Utopia Level 2 Plus Receive interface

AMP Mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor A pin 5	CLK0	RXFCSEO
Mictor C pin 7	C3:7	RXMSO
Mictor C pin 23	C2:7	RXABTO
Mictor C pin 9	C3:6	RXSOFO
Mictor C pin 11	C3:5	RXEOFO

Signals not Required for Disassembly

Tables 3–23 and 3–24 show the signals not required for disassembly of the Utopia2 bus signals.

Table 3-23: Signals not required for UTOPIA2TX support

AMP Mictor connector pin assignment	Section:channel	UTOPIA2TX signal name
Mictor C pin 25	C2:6	TxPrty
Mictor C pin 27	C2:5	TxClav3
Mictor C pin 29	C2:4	TxClav2
Mictor C pin 31	C2:3	TxClav1

Table 3-24: Signals not required for UTOPIA2RX support

AMP Mictor connector pin assignment	Section:channel	UTOPIA2RX signal name
Mictor C pin 25	C2:6	RxPrty
Mictor C pin 27	C2:5	RxClav3
Mictor C pin 29	C2:4	RxClav2
Mictor C pin 31	C2:3	RxClav1

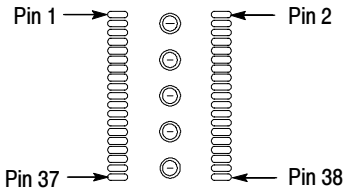
Signal Source To Mictor Connections

For design purposes, you may need to make connections between the Signal Source and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-XX, for more information on mechanical specifications. Tables 3–26 through 3–29 show the Signal Source to Mictor pin connections.

***NOTE**. To preserve signal quality in the target system, it is recommended that a 180 Ω resistor be connected in series between each ball pad of the Signal Source and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the Signal Source.*

The recommended pin assignment is the AMP pin assignment, because the AMP circuit board layout model and other commercial CAD packages use the AMP numbering scheme. See Table 3–25.

Table 3-25: Recommended pin assignments for a Mictor connector (component side)

Type of pin assignment	Comments
Recommended  **AMP Pin Assignment**	Recommended. This pin assignment is the industry standard and is what we recommend that you use.

Connections for Utopia2 Receive Interface

Tables 3–26 through 3–27 show the mictor pin connections for the Utopia2 Receive Interface.

Table 3-26: Signal Source to Mictor connections for Mictor A pins for UTOPIA2RX

AMP Mictor pin number	Logic analyzer channel name	UTOPIA2RX signal name
Mictor A pin 05	CLK0	RXFCSEO
Mictor A pin 07	A3:7	RxData15
Mictor A pin 09	A3:6	RxData14

Table 3-26: Signal Source to Mictor connections for Mictor A pins for UTOPIA2RX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA2RX signal name
Mictor A pin 11	A3:5	RxData13
Mictor A pin 13	A3:4	RxData12
Mictor A pin 15	A3:3	RxData11
Mictor A pin 17	A3:2	RxData10
Mictor A pin 19	A3:1	RxData9
Mictor A pin 21	A3:0	RxData8
Mictor A pin 23	A2:7	RxData7
Mictor A pin 25	A2:6	RxData6
Mictor A pin 27	A2:5	RxData5
Mictor A pin 29	A2:4	RxData4
Mictor A pin 31	A2:3	RxData3
Mictor A pin 33	A2:2	RxData2
Mictor A pin 35	A2:1	RxData1
Mictor A pin 37	A2:0	RxData0

Table 3-27: Signal Source to Mictor connections for Mictor C pins for UTOPIA2RX

AMP Mictor pin number	Logic analyzer channel name	UTOPIA2RX signal name
Mictor C pin 05	CLK3	RxClk
Mictor C pin 07	C3:7	RXMSO
Mictor C pin 09	C3:6	RXSOFO
Mictor C pin 11	C3:5	RXEOFO
Mictor C pin 13	C3:4	RxAddr4
Mictor C pin 15	C3:3	RxAddr3
Mictor C pin 17	C3:2	RxAddr2
Mictor C pin 19	C3:1	RxAddr1
Mictor C pin 21	C3:0	RxAddr0
Mictor C pin 23	C2:7	RXABTO
Mictor C pin 25	C2:6	RxPrty

Table 3-27: Signal Source to Mictor connections for Mictor C pins for UTOPIA2RX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA2RX signal name
Mictor C pin 27	C2:5	RxClav3
Mictor C pin 29	C2:4	RxClav2
Mictor C pin 31	C2:3	RxClav1
Mictor C pin 33	C2:2	RxEmpty*/RxClav
Mictor C pin 35	C2:1	RxSOC
Mictor C pin 37	C2:0	RxEnb*

Connections for Utopia2 Transmit Interface

Tables 3-28 through 3-29 show the mictor pin connections for UTOPIA2TX support.

Table 3-28: Signal Source to Mictor connections for Mictor A pins for UTOPIA2TX

AMP Mictor pin number	Logic analyzer channel name	UTOPIA2TX signal name
Mictor A pin 05	CLK0	---------
Mictor A pin 07	A3:7	TxData15
Mictor A pin 09	A3:6	TxData14
Mictor A pin 11	A3:5	TxData13
Mictor A pin 13	A3:4	TxData12
Mictor A pin 15	A3:3	TxData11
Mictor A pin 17	A3:2	TxData10
Mictor A pin 19	A3:1	TxData9
Mictor A pin 21	A3:0	TxData8
Mictor A pin 23	A2:7	TxData7
Mictor A pin 25	A2:6	TxData6
Mictor A pin 27	A2:5	TxData5
Mictor A pin 29	A2:4	TxData4
Mictor A pin 31	A2:3	TxData3
Mictor A pin 33	A2:2	TxData2
Mictor A pin 35	A2:1	TxData1
Mictor A pin 37	A2:0	TxData0

Table 3-29: Signal Source to Mictor connections for Mictor C pins for UTOPIA2TX

AMP Mictor pin number	Logic analyzer channel name	UTOPIA2TX signal name
Mictor C pin 05	CLK3	TxClk
Mictor C pin 07	C3:7	TXMSI
Mictor C pin 09	C3:6	TXSOFI
Mictor C pin 11	C3:5	TXEOFI
Mictor C pin 13	C3:4	TxAddr4
Mictor C pin 15	C3:3	TxAddr3

Table 3- 29: Signal Source to Mictor connections for Mictor C pins for UTOPIA2TX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA2TX signal name
Mictor C pin 17	C3:2	TxAddr2
Mictor C pin 19	C3:1	TxAddr1
Mictor C pin 21	C3:0	TxAddr0
Mictor C pin 23	C2:7	TXABTO
Mictor C pin 25	C2:6	TxPrty
Mictor C pin 27	C2:5	TxClav3
Mictor C pin 29	C2:4	TxClav2
Mictor C pin 31	C2:3	TxClav1
Mictor C pin 33	C2:2	TxFull*/TxClav
Mictor C pin 35	C2:1	TxSOC
Mictor C pin 37	C2:0	TxEnb*

Specifications

Specifications

This section contains the specifications for the support.

Specification Table

Table 4–1 lists the electrical requirements that the target system must produce for the support to acquire correct data.

Table 4–1: Electrical specifications

Characteristics	Requirements
Target system clock rate	
TMS822 specified clock rate	Maximum 50 MHz
TMS822 tested clock rate	Maximum 16.7 MHz
Minimum setup time required	
Logic analyzer	2.5 ns
Minimum hold time required	
Logic analyzer	0 ns

Replaceable Parts List

Replaceable Parts List

This section contains a list of the replaceable components and modules for the TMS822 UTOPIA2 support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

The tabular information in the *Replaceable Parts List* is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX, INC.	14150 SW KARL BRAUN DR P.O. BOX 500	BEAVERTON, OR, 97077-0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-1058-01			1	MANUAL,TECH INSTRUCTION,UTOPIA1/UTOPIA2;TMS822	80009	071-1058-01

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